Notice of Allowability	Application No.	Applicant(s)	
	10/635,379	MUNSHI ET AL.	
	Examiner	Art Unit	
	Michelle K. Lay	2672	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the application filed on 08/06/2003*.

2. ☒ The allowed claim(s) is/are *1-30*.

3. ☐ The drawings filed on _____ are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☒ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☒ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date 021005.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *021005 and 021505* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☒ Other *Drawing Corrections*.

MICHAEL RAZAVI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Themi Anagnos (Registration No. 47,388) on 02.15.2005. The application has been amended as follows:

[00019] Generally, the present invention includes a method and apparatus for graphics processing in a handheld device including a transform engine or vertex shader capable of receiving vertex information. The transform engine may be a fixed function transform engine capable of performing fixed function transformations of the vertex information or a programmable vertex shader. ~~-~~ Regardless thereof, the transform engine thereupon generates a plurality of vertices from the vertex information, wherein ~~the~~ each of the vertices includes a corresponding bin identifier. In one embodiment, the bin identifier is a multi-bit categorization of the associated vertex relative to its position on the screen.

[00022] As such, the present invention provides for ~~a~~ graphics processing in a handheld device by performing vertex transformations in two steps. The first step transforms the ~~vertex~~ vertices and outputs the transformed vertex buffer with a bin identifier and if the vertex is inside the clipping region writes the clip identifier. In the second step the

vertices are projected on to the screen using the view frame factors and the triangles are rendered. By breaking the vertex transformation into two steps this allows us to perform clipping on the CPU instead of on the graphics processor. Since the percentage of vertices that need clipping represent a very small number, this allows us to do clipping on the CPU without introducing too much additional overhead on the CPU and keep the gate count size down for the graphics processor which is extremely important since it affects power consumption. Another scarce resource is memory footprint available during rendering and it is possible that there will be configurations where we cannot allocate an entire Z, back buffer. This means that we need to break viewport rendering into multiple sub regions and render triangle lists into each of these regions. Since the same triangle list is being passed as input over multiple sub regions this results in wasted memory bandwidth since vertex data would have to be read multiple times (once for each sub-region) before deciding whether triangle is displayed in current sub-region and should be rendered or not. To reduce this memory bandwidth wastage the bin identifier is used. Instead of reading the vertex data first, we read the bin identifiers for vertices associate with a triangle. The vertex bin identifiers are used to determine if a triangle is displayed in current sub-region and if so then and then only the vertex data is read.

[00025] The vertex shader 102 thereupon determines if each of the vertices is within the viewable region by a comparison of the associated bin identifiers 110 with boundaries of the clipping region. For all vertices that are within the clipping region, a corresponding

clip identifier ~~112~~ 112a is generated. The clip identifier ~~112~~ 112a provides an indication of the vertex bin identifier 110 and other information for generating supplemental vertices ~~114~~ 118. The clip ~~identifier~~ identifiers ~~112~~ 112a and 112b ~~is~~ are discussed in further detail below with regards to FIG. 5.

[00026] Once all of the bin identifiers 110 have been compared with the clipping region, the clip identifiers ~~112~~ 112b are provided to a clipping module 116. In one embodiment, the clip identifiers 112a may be provided to a clip buffer 113 for intermediate storage therein, wherein the clip identifiers 112b may be further provided to the clipping module 116. In one embodiment, the clipping module 116 is a module implemented in software by a processor performing clipping operations in response to executable instructions. In one embodiment, the clipping module 116 receives the clip identifiers ~~112~~ 112b and generates supplemental vertices ~~114~~ 118 within the viewable region and/or outside of the clipping region, as illustrated in further detail in FIGS. 6-7 below. The supplemental vertices are appended into the vertex buffer.

[00030] FIG. 2 illustrates another embodiment 140 of the present invention including ~~the,~~ the vertex shader 102 and the clipping module 1 16. As described above, the vertex shader 102 receives the vertex data 106, generates the bin identifiers 110 and uses the view frame factors 108 to generate the clip identifiers ~~112~~ 112a. The clipping module 116 generates the supplemental vertices with clip identifiers ~~114~~ 118 and provides these vertices ~~114~~ 118 to the vertex shader 102. Thereupon the bin identifiers

and supplemental vertices 121 generated via the viewport transform engine ~~103~~ 104 are provided to a ~~set~~ set-up engine ~~152~~ 142.

[00031] FIG. 2 illustrates the pixel-processing pipeline used to process the vertex information within the vertex buffer 120. In one embodiment, the pixel processing pipeline operates in accordance with known pixel processing techniques using the set-up engine 142, a rasterizer engine ~~133~~ 144, a pixel operation module 146, a frame buffer 148 and a display 150. As described above, the vertex shader 102, upon executing the viewport transform, issues triangles 152 to the set-up engine 142. The set-up engine 142 generates the primitives 154 which are provided to the rasterizer engine 144, wherein the rasterizer engine 144 performs rasterization operations thereon. Upon generating a plurality of pixels 156, the pixel operation module 146 may thereupon perform any pixel operation, such as scaling, as recognized by one having ordinary skill in the art.

[00032] Thereupon, the pixel operation module 146 provides pixel output 158 to the frame buffer 148, which may be any suitable memory device as recognized by one having ordinary skill in the art. The frame buffer 148 receives the pixel output 158 and stores the pixel information therein. Once a frame has been saved in the frame buffer, a frame 160 is provided to the display. As the present invention provides for graphics processing in a handheld device, the display 150 may be a liquid crystal display, a small

flat panel display or any other suitable display as recognized by one having ordinary skill in the art being capable of being disposed within a handheld device.

[00042] FIG. 5 illustrates graphical representation of a clip ID 260 having a corresponding bin ID 250 and a vertex ID 262. As described above, when a vertex is determined to be clippable, such ~~a~~ as violating Z or X, Y region restrictions, the clip ID 260 is generated from the 8 bit bin ID 250 and the vertex ID 262. Although, as recognized by one having ordinary skill in the art, the bin ID 250 may be any suitable number of bits to provide for further scalability of the present invention, including scalability in the number of grids and assignment of a bin identifier per vertex allocation.

[00044] FIGS. 6 and 7 illustrate vertices before and after the clipping process. FIG. 6 illustrates a triangle 300 having three vertices, 302, 304 and 306. The clipping region 308 is defined as regions outside of the viewable area, in contradistinction to the viewable area 310. Based on graphics processing described above, an analysis of the vertices 302, 304 and 306 will provide for the generation of a clip ID ~~304~~ for the vertex 306. Whereas, vertices 302 are 304 are within the viewable area 310, so no clip IDs are generated for these vertices.

[00045] In accordance with one embodiment of the present invention, FIG. 7 illustrates the generation of supplemental vertices of 312 and 314 having corresponding bin identifiers. The supplement vertices 312 and 314 are generated within the viewable

region ~~310~~ 320 outside of the clipping region 308. Through a calculation of the intersection of the edge of clipping region 308 between the clip ID for vertex ~~304~~ 306 and the bin ID for vertex 302 provides for the location of the supplemental ~~vertices~~ vertex 314. Furthermore, a calculation of the location between the clip ID for vertex 306 and the bin ID for vertex 304 upon the intersection of the clipping region 308 provides for the supplemental ~~vertices~~ vertex 312. FIG. 7 illustrates the 2 newly generated triangles 316 and ~~318~~ 328 having vertices (302, 304, 312) and (302, 312, 314), respectively, within the display area and outside of the clipping region 308.

[00046] FIG. 8 illustrates one embodiment of the vertex shader 102 coupled to the CPU 206 and a clip counter 330, in accordance with one embodiment of the present invention. In one embodiment, the vertex data 106 of FIG. 1, starts in a main memory, such as the memory 208 of FIG. 3 and is written to an input buffer. In one embodiment, using matrix multiplication, the vertex data 106 may be received as a series of data bits having the vertex information in a sequential order. In one embodiment, the CPU 206 creates clippable versions of the vertex information to form the supplemental vertices which are thereupon added to the list of vertex information. In one embodiment, the vertex shader 102 includes a vertex data buffer 332 storing vertex data therein which is provided to a plurality of arithmetic logic units 334(a), 334(b), 334(n). The arithmetic logic units provide arithmetic operations such that the vertex data is transformed to be provided to an output buffer 336. The vertex shader 102 further includes a controller 338 which receives control information 340 from the vertex data 332 and provides

control information 342 to the output buffer 336 in accordance with known control techniques.

REASONS FOR ALLOWANCE

The following is an examiner's statement of reasons for allowance:

References Maillot (US Patent No. 5,079,719), Marion et al. (US Publication No. US 2004/0164999 A1), Kirkland (US Patent No. 5,986,669), Rossin et al. (US Patent No. 5,877,773) and Sutherland et al. ("Reentrant Polygon Clipping", Communication of the ACM, Volume 17, No. 1) are made of record as teaching the art of clipping for a predetermined size viewing area by detecting if the object, or portions of the object lay within the viewing region or the clipping region. However, none of the prior art teaches or suggests the use of a vertex shader that is capable of receiving a plurality of vertex information and generating vertices, where each of the vertices has a corresponding bin identifier. Furthermore, there is no suggestion that the vertex shader is coupled to a clipping module where the vertex shader provides the vertices having a corresponding clip identifier to the clipping module which then generates supplemental vertices, as claimed.

Conclusion

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michelle K. Lay whose telephone number is (571) 272-7661. The examiner can normally be reached on Monday - Friday, 7:00am - 3:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Razavi can be reached on (571) 272-7664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

mkl 02.15.2005

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